

AMENDMENTS TO THE CLAIMS

1-3. (Cancelled)

4. (Currently amended) ~~The wobble signal processing apparatus as defined in Claim 2 wherein~~ A wobble signal processing apparatus comprising:

a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal and a RF signal;

a WBL binarization circuit for smoothing edges of the wobble binary signal outputted from said pickup;

a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC;

a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal outputted from said pickup;

a phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data; and

a PLL (Phase Locked Loop) circuit, which is connected to said phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit;

wherein said address detection circuit and said waveform shaping circuit are digitally configured;

wherein said waveform shaping circuit includes a BPF (Band Pass Filter) as a digital filter, said digital filter being constituted by an IIR (Infinity Impulse Response) digital filter having a reset function of initializing said digital filter when characteristics of said digital filter are divergent; and

wherein said the digital filter calculates-is operable to calculate an optimum tap coefficient value, stores-store the optimum tap coefficient value in a storage unit that is externally provided, and performs-following-perform filtering by utilizing the optimum tap coefficient value stored in the storage unit.

5. (Currently amended) ~~The wobble signal processing apparatus as defined in Claim 1-A~~ wobble signal processing apparatus comprising:

a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal and a RF signal;

a WBL binarization circuit for smoothing edges of the wobble binary signal outputted from said pickup;

a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC;

a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal outputted from said pickup;

a phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data; and

a PLL (Phase Locked Loop) circuit, which is connected to said phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit;

wherein said address detection circuit and said waveform shaping circuit are digitally configured; and

wherein the-said address detection circuit comprises:

a digital filter for filtering the digital signal output-outputted from the said ADC; and

a PRML (Partial Response Maximum Likelihood) circuit for correcting errors in the signal outputted from the said digital filter, and detecting the ADIP signal by using the corrected signal.

6. (Currently amended) ~~The wobble signal processing apparatus as defined in Claim 5 wherein~~ A wobble signal processing apparatus comprising:

a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal and a RF signal;

a WBL binarization circuit for smoothing edges of the wobble binary signal outputted from said pickup;

a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC;

a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal outputted from said pickup;

a phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data; and

a PLL (Phase Locked Loop) circuit, which is connected to said phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit;

wherein said address detection circuit and said waveform shaping circuit are digitally configured;

wherein said address detection circuit comprises:

a digital filter for filtering the digital signal outputted from the said ADC;
and
a PRML (Partial Response Maximum Likelihood) circuit for correcting
errors in the signal outputted from said digital filter, and detecting the ADIP
signal by using the corrected signal; and
wherein a PRML system that is implemented by the said PRML circuit is a
PR(a,b) system.

7. (Currently amended) The wobble signal processing apparatus as defined in Claim 6, wherein parameter values in the PR(a,b) system have a relationship of $a=b$.

8. (Currently amended) ~~The wobble signal processing apparatus as defined in Claim 5 wherein~~ A wobble signal processing apparatus comprising:

a pickup for reading information recorded on an optical disc medium on/from
which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble
signal and a RF signal;

a WBL binarization circuit for smoothing edges of the wobble binary signal
outputted from said pickup;

a FEP (Front End Processor) for performing band limitation and gain control to
the wobble signal outputted from said pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted
from said FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal
as address information of the data based on the digital signal outputted from said ADC;

a waveform shaping circuit for generating a wobble binary signal waveform based
on the RF signal outputted from said pickup;

a phase control circuit for controlling the phase of the wobble binary signal
outputted from said WBL binarization circuit with reference to the wobble binary signal
waveform generated by said waveform shaping circuit, and outputting phase controlled
data; and

a PLL (Phase Locked Loop) circuit, which is connected to said phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit;

said address detection circuit and said waveform shaping circuit are digitally configured;

wherein said address detection circuit comprises:

a digital filter for filtering the digital signal outputted from said ADC; and

a PRML (Partial Response Maximum Likelihood) circuit for correcting errors in the signal outputted from said digital filter, and detecting the ADIP signal by using the corrected signal; and

wherein said PRML circuit is operable to switch a sampling method between a peak sampling method and an offset sampling method.

9. (Currently amended) The wobble signal processing apparatus as defined in Claim 8, wherein the said PRML circuit performs is operable to perform the sampling in a cycle of 8T.

10. (Currently amended) The wobble signal processing apparatus as defined in Claim 5 wherein A wobble signal processing apparatus comprising:

a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal and a RF signal;

a WBL binarization circuit for smoothing edges of the wobble binary signal outputted from said pickup;

a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC;

a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal outputted from said pickup;

a phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data; and

a PLL (Phase Locked Loop) circuit, which is connected to said phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit;

wherein said address detection circuit and said waveform shaping circuit are digitally configured;

wherein said address detection circuit comprises:

a digital filter for filtering the digital signal outputted from said ADC; and

a PRML (Partial Response Maximum Likelihood) circuit for correcting errors in the signal outputted from said digital filter, and detecting the ADIP signal by using the corrected signal; and

wherein said the PRML circuit performs is operable to perform a standardized Euclidean distance algorithm in a computing circuit of a Viterbi decoder by the PRML system.

11. (Currently amended) ~~The wobble signal processing apparatus as defined in Claim 1~~ wherein A wobble signal processing apparatus comprising:

a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal and a RF signal;

a WBL binarization circuit for smoothing edges of the wobble binary signal outputted from said pickup;

a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC;

a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal outputted from said pickup;

a first phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data; and

a PLL (Phase Locked Loop) circuit, which is connected to said first phase control circuit, for generating a sync clock based on the phase controlled data outputted from said first phase control circuit;

wherein said address detection circuit and said waveform shaping circuit are digitally configured; and

wherein said the-address detection circuit comprises:

a first digital filter for filtering the digital signal outputted output from the said ADC;

a second phase control circuit for controlling the phase of the wobble binary signal outputted from the said WBL binarization circuit with referring reference to the signal outputted from the said first digital filter, and outputting a phase controlled signal;

a multiplier for multiplying the signal outputted from the said first digital filter by the phase controlled signal outputted from said second phase control circuit;

a second digital filter for filtering an output from the said multiplier;

an edge smoothing circuit for binarizing the signal outputted from the said first digital filter, and smoothing edges of the binarized signal, thereby generating so as to generate a clock for outputting the ADIP signal; and

a binarization circuit for binarizing the signal outputted from the said second digital filter in accordance with the clock that is outputted from the said edge smoothing circuit, and outputting the ADIP signal.

12. ~~(Currently amended) The wobble signal processing apparatus as defined in Claim 1 wherein~~ A wobble signal processing apparatus comprising:

a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal and a RF signal;

a WBL binarization circuit for smoothing edges of the wobble binary signal outputted from said pickup;

a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC;

a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal outputted from said pickup;

a phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data; and

a PLL (Phase Locked Loop) circuit, which is connected to said phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit;

wherein said address detection circuit and said waveform shaping circuit are digitally configured;

wherein said waveform shaping circuit includes a digital filter for generating the wobble binary signal waveform based on the RF signal outputted from said pickup; and

wherein said the-phase control circuit obtains-is operable to obtain a phase difference between the wobble binary signal and the wobble binary signal waveform that has passed through the-said digital filter, and ~~controls-control~~ the phase by delaying the wobble binary signal.

13. (Currently amended) The wobble signal processing apparatus as defined in Claim 12, wherein said the phase control circuit corrects-is operable to correct a phase shift by performing counter processing to clock delay information previously obtained.

14. (Currently amended) ~~The wobble signal processing apparatus as defined in Claim 1 wherein~~ A wobble signal processing apparatus comprising:

a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal and a RF signal;

a WBL binarization circuit for smoothing edges of the wobble binary signal outputted from said pickup;

a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC;

a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal outputted from said pickup;

a phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data; and

a PLL (Phase Locked Loop) circuit, which is connected to said phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit;

wherein said address detection circuit and said waveform shaping circuit are digitally configured; and

wherein said the address detection circuit comprises:

a digital filter for filtering the digital signal outputted output from the said ADC; and

a DSV (Digital Sum Value) calculator for digitally processing the output from the said digital filter by dividing the output from said digital filter same with a predetermined threshold value, thereby detecting so as to detect the ADIP signal.

15. (Currently amended) ~~The wobble signal processing apparatus as defined in Claim 1 wherein~~ A wobble signal processing apparatus comprising:

a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal and a RF signal;

a WBL binarization circuit for smoothing edges of the wobble binary signal outputted from said pickup;

a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC;

a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal outputted from said pickup;

a phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data; and

a PLL (Phase Locked Loop) circuit, which is connected to said phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit;

wherein said address detection circuit and said waveform shaping circuit are digitally configured;

wherein said the address detection circuit comprises:

a digital filter for filtering the digital signal outputted output from the said ADC;

a binarization circuit for binarizing the output from the said digital filter;
and

a counter circuit for counting ~~the a~~ number of +1 and ~~the a~~ number -1 in the signal outputted from the said binarization circuit; and

wherein said address detection circuit is operable to detect the ADIP signal is detected based on the basis of the count values of the said counter circuit.

16. (Currently amended) The wobble signal processing apparatus as defined in ~~Claim~~ 1 Claim 12, wherein the said ADC has a 7-bit resolution.

17. (Currently amended) ~~The wobble signal processing apparatus as defined in Claim~~ 1 wherein A wobble signal processing apparatus comprising:

a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal and a RF signal;

a WBL binarization circuit for smoothing edges of the wobble binary signal outputted from said pickup;

a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC;

a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal outputted from said pickup;

a phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data; and

a PLL (Phase Locked Loop) circuit, which is connected to said phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit;

wherein said address detection circuit and said waveform shaping circuit are digitally configured;

wherein said the-FEP further includes an AGC (Auto Gain Control) circuit for performing automatic amplitude control when the an amplitude of a section of the ADIP section-signal is decreased or increased due to crosstalk in the optical disc medium.

18. (Currently amended) ~~The wobble signal processing apparatus as defined in Claim 1~~ wherein A wobble signal processing apparatus comprising;

a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal and a RF signal;

a WBL binarization circuit for smoothing edges of the wobble binary signal outputted from said pickup;

a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC;

a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal outputted from said pickup;

a phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data; and

a PLL (Phase Locked Loop) circuit, which is connected to said phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit;

wherein said address detection circuit and said waveform shaping circuit are digitally configured; and

wherein said the pickup further includes an aperture ratio decision unit for deciding the a degree of distortion of the a waveform that is read from the optical disc medium, and controls said pickup is operable to control a the diameter of a beam spot of a pickup laser based on the basis of the decided degree of distortion of the waveform, thereby controlling so as to control the degree of signal component extraction.

19. (Currently amended) The wobble signal processing apparatus as defined in Claim 1-Claim 12, wherein:

said apparatus operates in accordance with the sync clock that is supplied from the generated by said PLL circuit; and

the sync clock is adaptively changed according to an angular velocity of the optical disc medium.

20. (Currently amended) The wobble signal processing apparatus as defined in Claim 3 wherein A wobble signal processing apparatus comprising:

a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal and a RF signal;

a WBL binarization circuit for smoothing edges of the wobble binary signal outputted from said pickup;

a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup;

an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal;

an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC;

a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal outputted from said pickup;

a phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data; and

a PLL (Phase Locked Loop) circuit, which is connected to said phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit;

wherein said address detection circuit and said waveform shaping circuit are digitally configured;

wherein said address detection circuit includes a LPF (Low Pass Filter) as a digital filter, said digital filter being constituted by an IIR digital filter having a reset function of initializing said digital filter when characteristics of said digital filter characteristics are divergent; and

wherein said the-digital filter calculates-is operable to calculate an optimum tap coefficient value, stores-store the optimum tap coefficient value in a storage unit that is externally provided, and performs-following-perform filtering by utilizing the optimum tap coefficient value stored in the storage unit.

21. (Currently amended) The wobble signal processing apparatus as defined in Claim 11, wherein:

said waveform shaping circuit includes a digital filter for generating the wobble binary signal waveform based on the RF signal outputted from said pickup; and

the-said phase control circuit is operable to obtain obtains-a phase difference between the wobble binary signal and the wobble binary signal waveform that has passed through the-said digital filter, and controls-control the phase by delaying the wobble binary signal.

22. (Currently amended) The wobble signal processing apparatus as defined in Claim 21, wherein the-said phase control circuit is operable to correct corrects-a phase shift by performing counter processing to clock delay information previously obtained.